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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/581,024	04/12/2007	Atsuhiro Mori	061282-0202	7399

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MCDERMOTT WILL & EMERY LLP
600 13TH STREET, NW
WASHINGTON, DC 20005-3096

EXAMINER	
TAN, VIBOL	
ART UNIT	PAPER NUMBER
2819	
MAIL DATE	DELIVERY MODE
06/20/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/581,024	MORI ET AL.	
	Examiner	Art Unit	
	Vibol Tan	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 April 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-16* is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 May 2006* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *5/30/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, ***transistors higher in threshold voltage in claim 10; and said second logical elements have a layout structure different from that of said first logical elements in claim 11*** must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claim 11 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

4. In claim 11, it is not clearly defined wherein said second logical elements have a layout structure different from that of said first logical elements since different layout structures between the two logical elements would result in different logic which in turn contradicts with what previously recited in claim 9, as the second logical elements having the same logic as said the first logical elements.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 9, 13 and 16 are rejected under 35 U.S.C. 102(e) as being anticipated by New (US 2004/0174187).

In claim 9, New teaches all claimed features a programmable logic device comprising an array of programmable logical elements (logical elements reside in each

CLB, Fig. 3), said programmable logic device characterized in that said logical elements include: first logical elements (logical elements in a CLB 301a) having a predetermined logic (logical function); and second logical elements (other logical elements in the CLB 301) having the same logic as said first logical elements but having an upper limit (maximum speed limit) of operating speed designed to be lower (slower for low power consumption [0012]) than that of said first logical elements.

In claim 13, New further teaches the programmable logic device of claim 9, wherein said first logical elements are arranged collective in one place (not shown, the logical elements reside in the CLB 301a are arranged in one place).

Method claim 16 corresponds to detailed circuitry already discussed similarly with regard to claim 9.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 10, 12, 14 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over New.

In claim 10, New teaches all claimed features the programmable logic device according to claim 9; with the exception of teaching wherein each of said second logical elements uses transistors higher in threshold voltage compared with transistors used in each of said first logical elements. However, New teaches in paragraph [0013] the

interconnect resources in the set include a set of first transistors, while the interconnect resources in the second set include a set of second transistors. The first transistors have a lower effective threshold voltage than the second transistors. Thus, it would have been obvious to implement the same teachings for the second logical elements uses transistors higher in threshold voltage compared with transistors used in each of said first logical elements.

Therefore; it would have been obvious to one ordinary skill in the art at the time of the invention was made to implement the teachings of New for the second logical elements uses transistors higher in threshold voltage compared with transistors used in each of said first logical elements, in order to provide a PLD with high speed and low power consumption.

In claim 12, New teaches all claimed features the programmable logic device according to claim 9; with the exception of teaching wherein the first logical elements are operated by a clock signal with a first clock frequency; and said second logical elements are operated by a clock signal with a second clock frequency lower than said first clock frequency. However, it is obvious to operate the first logical elements with a clock signal having a first clock frequency, and the second logical elements with a second clock signal having a second clock frequency since the first and second logical elements operate at different speeds.

Therefore; it would have been obvious to one ordinary skill in the art at the time of the invention was made by implementing the first logical elements to be operated by a clock signal with a first clock frequency and the second logical elements by a clock

signal with a second clock frequency lower than the first clock frequency, in order to provide a PLD with high speed and low power consumption.

In claim 14, New teaches all claimed features the programmable logic device according to claim 13; with the exception of teaching wherein said first logical elements are arranged in a center portion of said programmable logic device; and said second logical elements are arranged in a peripheral portion of said programmable logic device with respect to the region where said first logical elements are arranged. However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to arrange said first logical elements to be in a center portion of said programmable logic device and said second logical elements to be in a peripheral portion of said programmable logic device with respect to the region where said first logical elements are arranged, since it has been held that rearranging parts of an invention involves only routine skill in the art. *In re Japikse,* 86 USPQ 70.

Therefore; it would have been obvious to one ordinary skill in the art at the time of the invention was made to arrange the locations of the first and second logical elements, as a matter of engineering design choice based on system involved.

Claim 15 is rejected in the same manner as claim 14.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vibol Tan whose telephone number is (571) 272-1811. The examiner can normally be reached on Monday-Friday (7:00 AM-4:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rexford Barnie can be reached on (571) 272-7492. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Vibol Tan/
Primary Examiner
Art Unit 2819